Symposium on Experiences of porting and optimising code for Xeon Phi processors

Session 1: 11.30 – 12.30
Chair: Michele Weiland
● 11.30 Introduction and welcome
  ● Michele Weiland, EPCC
● 11.40 Experiences optimising applications for the Xeon Phi
  ● Andrew Mallinson, Intel

Session 2: 14.00 – 15.30
Chair: Michele Weiland
● 14.00 Preparing a Seismic Imaging Code for the 'Intel Knights Landing
  ● Gilles Civario, ICHEC
● 14.30 Experiences porting production codes
  ● Fiona Reid, EPCC
● 15.00 Optimisation of Unified Model Radiation Calculation
  ● Luke Mason, STFC

Session 3: 16.00 – 17.30
Chair: Andrew Mallinson
● 16.00 Grid: A data parallel library for Cartesian mesh PDE problems.
  ● Peter Boyle, University of Edinburgh
● 16.40 Evaluating OpenMP's nested parallelism on Xeon Phi
  ● Mike Boulton, Bristol University
● 17.00 DualSPHysics Performance on Xeon Phi
  ● Sergi Siso, STFC